REMARKS

Applicants thank Examiner Corrielus for the courtesy of conducting a telephone interview on December 14, 2006, during which the pending claims and the cited references were discussed.

Support for the amendments to the specification can be found in the originally-filed application filed on June 21, 2001, which included a paragraph at the beginning of the specification claiming priority to Provisional U.S. Application Serial No. 60/213,349. Furthermore, amendments to the specification remove reference to an Appendix, which does not exist in the application, and an extraneous comment, and do not add new matter.

Claims 1, 3, 4, and 10-13 are rejected under 35 U.S.C. § 103(a) over U.S. Patent No. 5,920,873 to Van Huben ("Van Huben") and U.S. Patent No. 6,161,211 to Southgate ("Southgate"), and those claims also are rejected under 35 U.S.C. § 103(a) over Van Huben and U.S. Patent No. 5,920,873 to Dole ("Dole").

Without prejudice, and without acknowledging agreement with or acquiescence to the rejections to the claims, applicants hereby amend claims 1 and 3. Applicants submit that all of the claims pending after entry of this paper (i.e., claims 1, 3, 4, and 10-13) are in condition for allowance. Support for the claim changes can be found throughout the published substitute specification filed January 18, 2002, and at, for example, page 12, lines 25-30 through page 13, lines 1-2, and FIG 3A. Also, support for the claim changes can be found throughout the priority Provisional U.S. Patent Application Serial No. 60/213,349 on page 5, line 27, page 6, lines 2-3 and lines 41-45, and page 8 lines 53-55.

As indicated in the background section of applicants' specification, existing software applications generate intelligent design data and save it in particular and different file formats. Unlike existing applications, a single software application with an automatic format verifier can automatically determine the specific format of any intelligent design data file and automatically

identify from a library of format readers an appropriate format reader that is capable of reading that specific file format, all without any user intervention.

Furthermore, the single software application includes format writers for saving into a single export data file the different data files loaded into the single software application. Once created, the export data file can be loaded back into the single software application to facilitate design collaboration among multiple design groups working on various aspects and phases of the intelligent design.

Van Huben is completely silent about an automated format verifier, format writers, and an export data file. Southgate fails to cure this defect in Van Huben. Instead, Southgate discloses a design methodology by which designers can create, test, and optimize circuit designs. (See Southgate, at col. 3, lines 19-22.) Designers can create a design hierarchy of a circuit design, which includes a high-level block diagram of a circuit design, and sublevels defining details of each block in the circuit design. (See Southgate, at col. 3, lines 19-26.) Designers use a graphic editor to create the high-level block diagram of the circuit design. (See Southgate, at col. 3, lines 36-39.) For each block in the high-level diagram, designers can use a text or graphic editor to create and define the block. For example, designers may use a text editor to define a block in Verilog, or a graphic editor to define a block using a visual representation. (See Southgate, at col. 3, lines 39-50.) Each block is saved in a separate design file, which may be in a variety of existing formats for storing circuit designs. Id.

In Southgate, designers can test and optimize the circuit design. The design files are translated into a user design netlist for use with a compile flow manager for testing and optimizing the design. (See Southgate, col 8., starting at line 27, through col. 9, line 12, and FIG. 4.) If the circuit design does not operate correctly, designers can make changes in a design file, which are automatically incorporated into affected design files representing blocks at other levels of the circuit design. (See Southgate, at col. 3, lines 50-53, and FIG 1, 132.)

Southgate is completely silent at least about a single software application comprising an automated format verifier. Furthermore, Southgate is completely silent about format writers and

an export data file. Accordingly, a prima facie case of obviousness does not exist with the combination of Van Huben and Southgate.

Dole also fails to cure the defects of Van Huben. Dole discloses the use of a format converter utility "to convert the output file to a format acceptable to the application." (See col. 8, lines 21-37, and FIG. 6, 2300, 2303, 2305, 2307, and 2309.) As an example, Dole discloses the use of a converter with an XML parsing capability for converting an electronic design file into multiple files. (See col. 16, lines 50-55, and FIG. 13.) Dole does not teach or suggest at least a single software application comprising an automated format verifier. Furthermore, Does does not teach or suggest format writers and an export data file. Accordingly, a prima facie case of obviousness also does not exist with the combination of Van Huben and Dole.

Applicants note that pages 5 and 8 of the action reference Heile in rejecting claims 4, 10, 11, 12, and 13, but Heile is not being relied upon to reject any of the claims according to pages 3 and 6 of the action. Applicants assume that Heile was mistakenly referenced instead of Southgate (page 5) and Dole (page 8). The column and line number references on pages 5 and 8 do not seem to relate to Southgate and Dole, respectively.

CONCLUSION

In view of the foregoing, applicants request entry and consideration of this paper and allowance of all pending claims (i.e., claims 1, 3, 4, and 10-13) in due course.

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Respectfully submitted,

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